ABSTRACT

A testing unit (10) for testing a device under test – DUT – (30) comprises a signal generator (20) for applying a stimulus signal to the DUT (30), a receiving unit (50) for receiving a response signal from the DUT on the applied stimulus signal, and a synchronizing unit (40) for synchronizing a data flow of the response signal between the DUT (30) and the receiving unit (50). The synchronizing unit (40) receives a first clock signal (DUT-CLK) from the DUT (30) and a second clock signal (CLK) of the testing unit (10). The synchronizing unit (40) comprises a buffer (70) for buffering data, a write unit (80) for writing data from the DUT (30) into the buffer (70), and a read unit (90) for reading out data from the buffer (70) to be provided to the receiving unit (50). A write access onto the buffer (70) is controlled by the first clock signal (DUT-CLK), while a read access onto the buffer (70) is controlled by the second clock signal (CLK).

[Fig. 1 for publication]